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The hidden connections between SI and PI

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Signal integrity (SI) gradually became a topic on its own right and grew out of the electromagnetic compatibility (EMC) discipline in the 90s. About a decade later power integrity (PI) also became a hot topic and created a separate discipline with multitude of books and conference sessions devoted to it. Originally, SI was based on high-frequency RF and microwave knowledge, whereas PI tasks were handled by AC-DC and DC-DC power supply designers, who primarily care for the low-frequency behavior of circuits. Though it has been understood all along that the same basic physics rules and principles apply to both SI and PI, the separate high-frequency and low-frequency considerations led to seemingly disconnected design rules.

Take for instance three-dimensional (3D) effects. We usually associate 3D effects with high-frequency SI situations, where the full-wave solution of Maxwell equations becomes necessary. This can happen for instance when we analyze a right-angle turn in a printed-circuit board (PCB) trace or look at the high-speed behavior of a plated through hole (PTH). In SI, the full-wave effects become noticeable at higher frequencies, where the physical dimensions are not negligibly small compared to the wavelength. Based on this it may be surprising to realize that in PI 3D effects equally show up, even at very low frequencies, sometimes in the kHz region. These 3D effects are created by changes in current density in conductors. An example of this behavior was documented by measured and simulated data in [1], where the conductor geometry and the component placement interacted in a way that created a negative phase and negative slope of magnitude of the impedance. Shown in Figure 1, the circuit in question was a small fixture, consisting of two coaxial connectors and four surface-mount resistors.

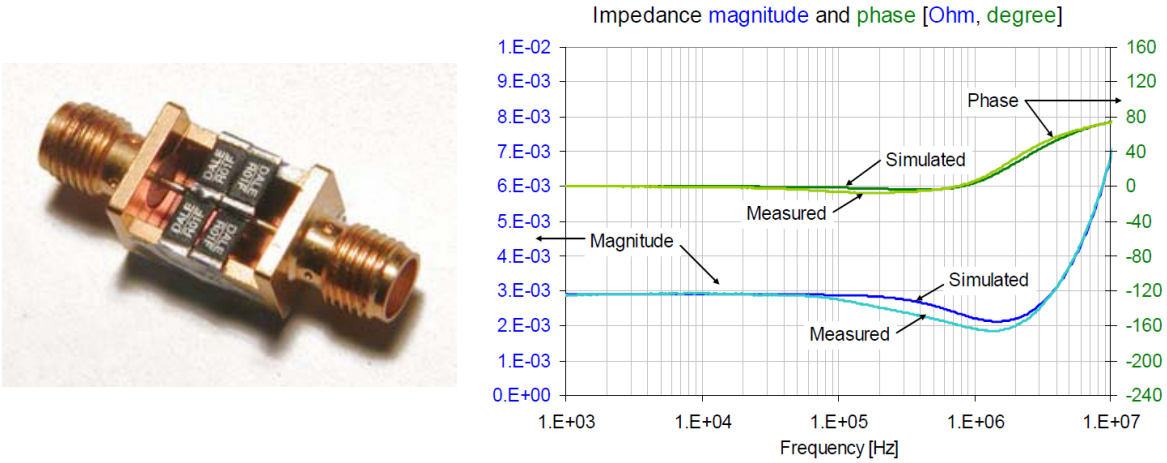

Figure 1: Small fixture with two coaxial connectors and resistors on the left, measured and simulated impedances on the right (after [1])

A recent illustration of another 3D effect showing up at relatively low frequencies was included in [2]. Figure 2 shows a computer rendering of two wafer probes measuring a chip's core power supply across two adjacent power-ground via pairs in a 1-mm array. The inductive coupling between the two loops formed by the probe tips has to be removed from the measured data. The coupling can be characterized on appropriate calibration substrates and the mutual inductance is shown on the right for three probe tip geometries. Note that the mutual inductance has different frequency dependency at low frequencies for the three probe geometries.

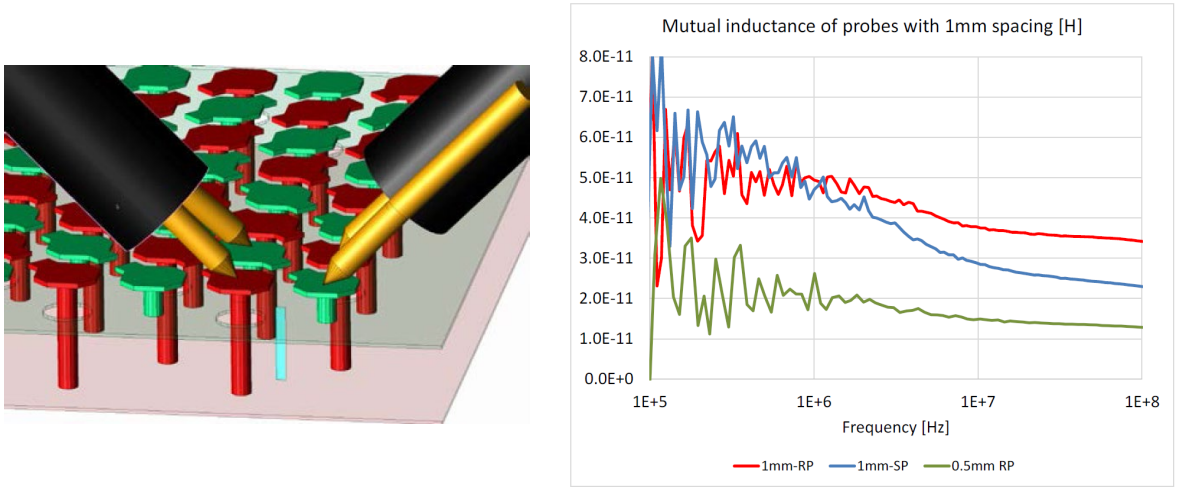

Figure 2: Wafer probe landing on a via-grid array (on the left) and the mutual inductance between the probe-tip loops as a function of frequency (on the right).

The above examples illustrate how high-frequency SI disciplines can show up somewhat unexpectedly in low-frequency PI characterization. But the opposite is also true: well-understood PI behavior could also turn up in our SI characterization data. Take for instance the cable-braid loop error that limits our dynamic range in low-frequency low-impedance PI measurements. An illustration of this is shown in Figure 3.

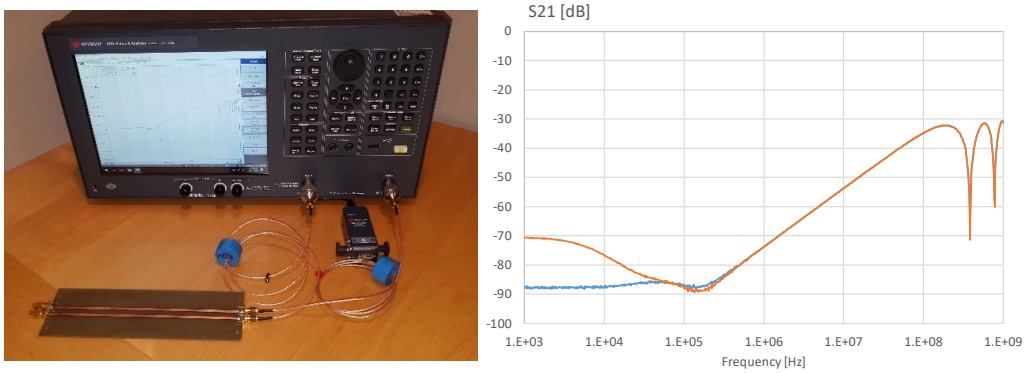

Figure 3: Near-end crosstalk between two microstrip traces. Left: setup photo. Right: measured crosstalk with and without cable-braid error reduction.

The illustrations above are just simple examples how SI and PI rules go hand in hand even if sometimes the SI or PI applications are unexpected and less studied. There and several other hidden connections between SI and PI, for instance how anisotropy also shows up at very low frequencies, even at DC.

These hidden connections are shown and discussed in two of my courses at University of Oxford: *Resetting Your Signal Integrity Knowledge* and *Making Successful Power Distribution Designs.*

References:

[1] "Accuracy Improvements of PDN Impedance Measurements in the Low to Middle Frequency Range," DesignCon 2010, February 1-4, 2010, Santa Clara, CA

[2] "3D Connection Artifacts in PDN Measurements," DesignCon 2023, January 30 – February 2, 2023, Santa Clara, CA

[3] "How the Braid Impedance of Instrumentation Cables Impact PI and SI Measurements," DesignCon 2019, January 29-31, 2019, Santa Clara, CA