How PCB Manufacturing and Assembly Details Affect SI and PI Board Performance

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In signal and power integrity (SI and PI) we ultimately would like to see reasonable agreement between the predicted, or simulated and the measured performance of our circuits. Real world measurements will always contain errors and they usually show a distorted replica of the true behavior of the Device Under Test (DUT). Real measurements always show more than just the behavior of the DUT. Even if we don't consider random noise and random errors, in the measured data we have contribution from instrument, cable and probe errors (just to name a few) that our calibration could not completely remove.

Simulations work differently: they always show less, an incomplete picture of the DUT, simply because practically there is no way for us to include every detail in our models. Not to mention the details that we may not even know about. In simulations our first question is how to select and set up the models and how to adjust the simulation tool settings so that we get the 'correct' and 'expected' results. But simulations will include only those details that we set up and specify in our simulation model. This is true for relatively well-known parameters, such as for instance the dielectric constant and loss tangent of laminates and also true for other parameters that we tend to describe with a range or with fitted models, such as surface roughness. Dimensional tolerances fall into this category. Dimensional tolerances can be considered in simulations, for instance by doing statistical margining of the dimensions. However, in high-speed interconnects there are so many geometry details that determine the channel performance that simulating a meaningful number of combinations become daunting. An interesting such case is related to backdrilling the unwanted via stub on high-speed channels. If the backdrilled hole is not concentric to the via barrel that we want to remove, there is a chance that a sliver of the barrel remains, illustrated with two photos in Figure 1.

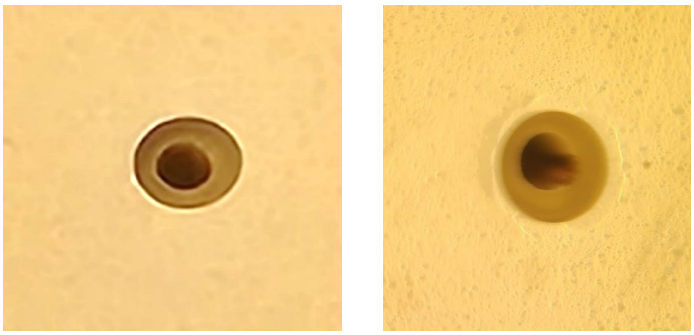

Figure 1: *Photos of 'good' and 'bad' backdrilling*

The photo on the left shows a properly backdrilled via. On the right, there is a visible misregistration of the backdrilled hole, leaving part of the original via barrel in place. The residual via barrel behaves similarly to a full via barrel; it creates a dip in the signal transmission. The frequency of the dip is inversely proportional to the length of residual barrel and the depth and bandwidth of the dip depend on its shape. Usually, narrower residual sliver means narrower dip on the frequency plot.

Though this is clearly a manufacturing defect, it does happen occasionally, because optical inspection of a high-aspect ratio small hole is challenging. The length, width and shape of any remaining barrel is highly statistical in such cases and correlation can only be successful if we first find the defect and get the dimensions of the remaining barrel by further analysis.

The next example, shown in Figure 2, is not the result of manufacturing defect: it can happen in any high-speed board. The case study in [1] described the impact of registration tolerances on connectorized differential pairs. Coaxial connectors today tens to be much bigger than our typical trace width in high-density high-speed boards, requiring us to start with uncoupled traces until we can bring the two traces closer to form a differential pair. This inevitably means that the immediate vicinity of the connector launch -though may be mirror image of each other- will not be identical. The close-up photo of the launch via shows a case where the manufacturing tolerance pushed the via barrel sideways, further away from the exiting trace. We can then expect (as it was verified) that the via barrel in the other launch will get closer to the exiting trace. This minute difference is enough to create the highlighted difference in the TDR response. For such cases the suggested solution of the cited reference is to exit differential launches with short parallel trace sections before the traces take a turn.

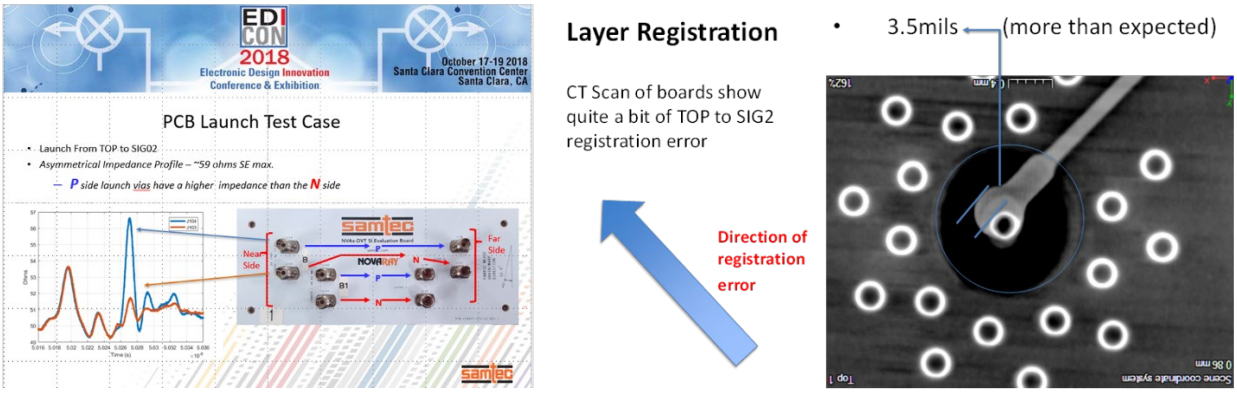

Figure 2: *Effect of misregistration on differential escape (reproduced from [1])*

The third illustration, related to assembly, is reproduced from [2] and it is shown in Figure 3. Many of our complex packages today use Ball Grid Array (BGA) connection to the printed circuit board. These tiny solder balls are usually placed on a regular grid with a center-to-center spacing that we call the pitch. For big chips 0.8mm and 1.0mm pitches may be common. For smaller packages and higher speeds smaller pitches are available.

When we route differential pairs though a package, it is a good idea to place the balls connecting the two legs of the differential pair on adjacent grid points and surround them with enough return ('ground') vias.

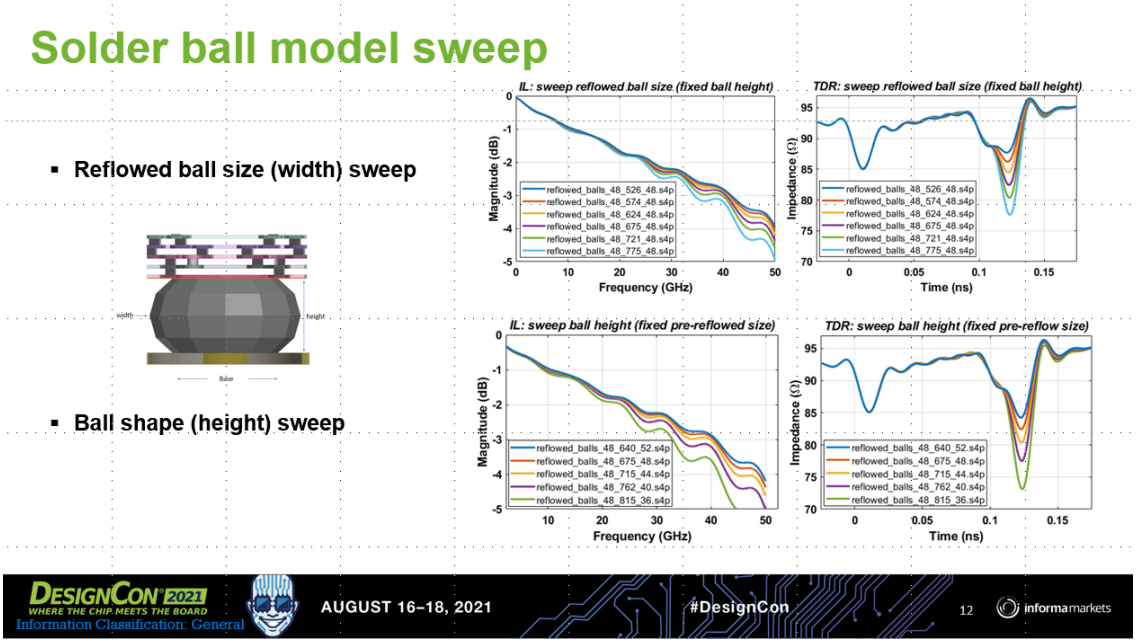

Figure 3: *Effect of solderball height on insertion loss and TDR profile (reproduced from [2])*

Return vias help to keep the impedance better defined through the transition between the board and package and provide isolation to and from nearby signal and power connections. During the solder reflow process, dependent on many factors, the size and shape of the solder balls will end up to be slightly different. These solder balls, no matter how tiny they look, still tend to be bigger than the connecting via barrels and traces and therefore seemingly small absolute variations in geometry numbers may result in very noticeable impedance, insertion loss and crosstalk performance differences. Reproduced from [2], Figure 3 shows the simulated performance as a function of solder ball dimensions.

Our final illustrations are related to power distribution. As opposed to the early days of electronic circuits, when carrying the power and ground connections around a board was done with wires or fat traces, to feed power-hungry chips consuming tens and hundreds of amperes, today we use power planes in our boards. When we define our stackup, the number and thickness (weight) of our power and ground layers, it is very useful to know a little bit about the processes how printed circuit boards are fabricated.

To determine the current-carrying capability of a power-plane shape, we need to know the thickness and conductivity of the copper, but instead of thickness and conductivity, in the trade of copper foils people use weight (you may hear people speaking about one ounce, or two ounce copper) and method of production (electro-deposited or rolled-annealed

copper). The recent "Mind Your Units" article [3] is a reminder that units matter and the units used for PCB fabrication and trade may be counter-intuitive to some people.

The way how the PCB copper is patterned during fabrication will also influence the current-carrying capability. During the wet etching process, the side walls of traces and plane shapes will become tilted. On a single large plane shape this may matter very little, but when we have large chips in a dense printed circuit board, we will end up with a lot of perforation due to the many antipads around vias that do not connect to the particular plane. This becomes obvious under the cores of big chips, where alternating power and ground through vias perforate the planes. If we do not take into account the slanted side walls, we may end up with a too optimistic design. The illustration in Figure 4 is reproduced from [4]. It shows the simulated voltage drop on the power plane of a high-current CPU rail, assuming vertical slide walls and the more typical; 60-degree side walls. The etch factor alone results in a 10% increase of end-to-end resistance. And that is on top of the impact of the perforation itself.

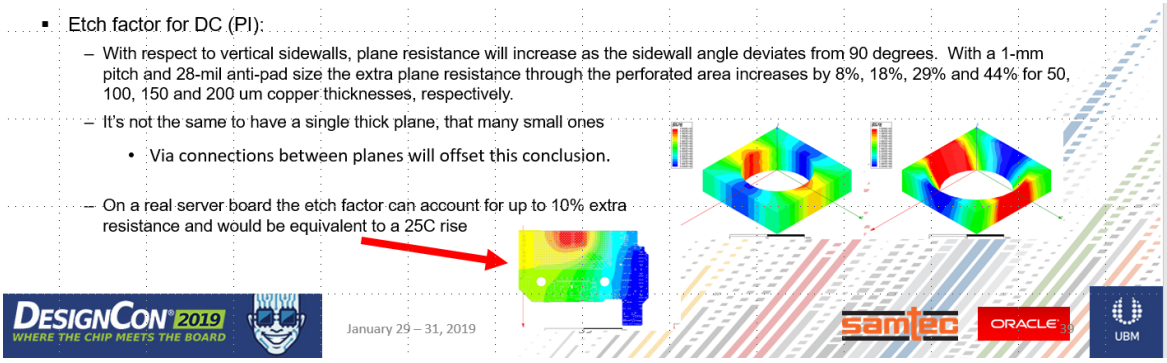

Figure 4: *Effect of etch factor on DC resistance and loss (reproduced from [4])*

Summary

We need to be aware of the basics of the PCB fabrication and assembly, because they have an impact on the high-speed, power integrity and thermal performance of our boards.

References:

[1] "Increasing Broadband Interconnect Characterization," EDICON 2018

[2] "A Case Study in the Development of 112 Gbps-PAM4 Silicon and Connector Test Platform,: DesignCon 2021

[3] "Mind Your Units," Printed Circuit Design and Fab, Circuit Assembly, December 2023, p. 56

[3] "Etch Factor Impact on SI & PI," DesignCon 2019