# Introducing an Upcoming IEEE Packaging Benchmark

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Introduction, background

In recent years the IEEE Electrical Packaging Society (EPS) technical committee on electrical design, modeling, and simulation (TC-EDMS) realized and recognized the need for open-source benchmarks for the simulation tool vendors, verification, test and measurement solution vendors. The intention is to overcome the obstacles that developers and users of such tools and instruments often have, and create a growing library of benchmark cases for signal and power integrity challenges [1], [2]. As of October 2023, there are four published benchmark cases in the repository. This document describes a proposal for a fifth benchmark.

This benchmark is based on the simulation and measurement challenges and test board features that are described in [3] and [4].
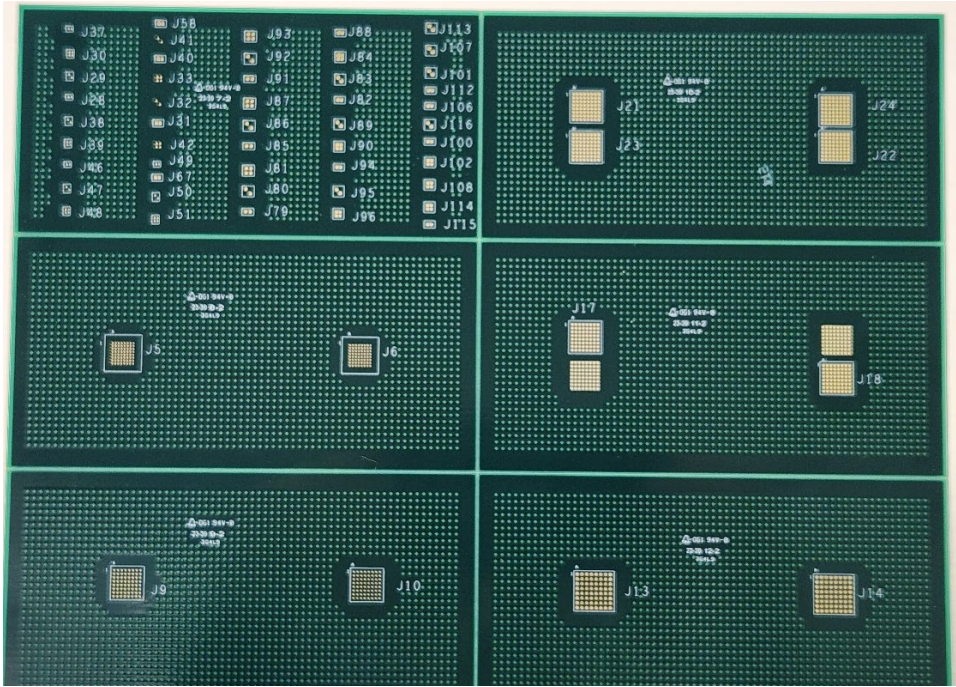

Front-view photo of the manufactured benchmark board, described in this document.

Purpose

The overall purpose of this board is to provide the industry with an open-source common test platform that is available to users, that can be built by the users if they wish and CAD companies can use to compare simulation tools, simulation setups across different types of simulators and simulators from different CAD companies, as well as allow instrument vendors to refine measurement, calibration and de-embedding solutions and eventually come to a reasonable correlation between simulated and measured values. A common open-source hardware platform allows various CAD and instrumentation companies to compare their results without sharing confidential details.

Specifically, the intended use of this benchmark test board is to facilitate the investigation of three areas: analyze the impact of probe-tip coupling in wafer probe calibrations and measurements, to investigate the impact of via coupling within the DUT and to better understand the spatial effects associated with large via arrays in low-impedance power distribution networks. The associated pieces in a PDN are illustrated in *Figure 1*.
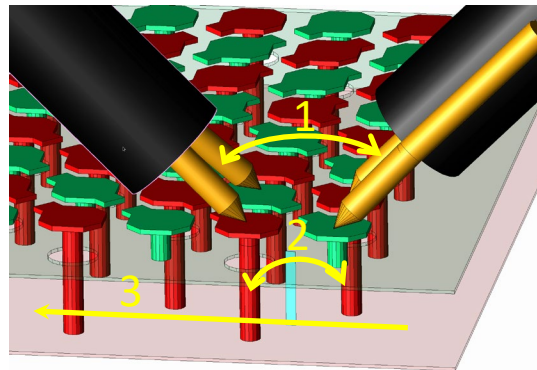
Figure 1.: *3D rendering of two single-ended wafer probes touching down on the corner of a large via array, illustrating the three possible areas of investigations: 1) probe-tip coupling, 2) via-loop coupling and 3) spatial effects (from [3]).*

What this benchmark board is *not* intended for:

- this board is designed for wafer-probe connections, *not* for direct coaxial connection.
- the board is also *not* intended for high-frequency modeling, high-frequency correlation, or high-frequency laminate characterization.
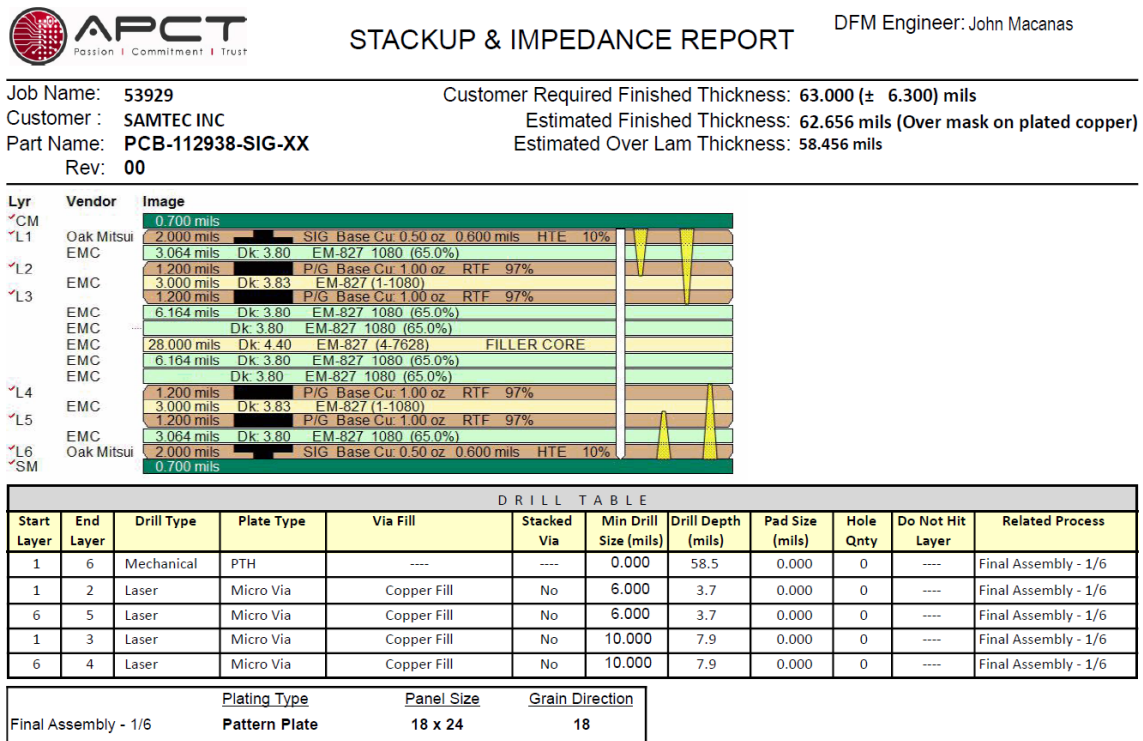
Description of the board

The board has six metal layers and can be built with low-cost foil construction lamination, with low-cost laminate materials. The same stackup can also be built with different laminates, not only with the one described here. Note that some of the power-ground laminates, especially the very thin ones may require sequential lamination process, required by the laminate itself.

The 10"x7.5" board is divided into six identical-size rectangular areas or sections. As described in detail later, each rectangular section has full planes within and only within their own boundaries, on all of their four internal core layers. The TOP and BOTTOM layers are pad only.

Stackup

The default board stackup, used for the first build, is shown on a PCB fab vendor drawing in *Figure 2*. The electrical properties used for simulations are shown later in the Simulation section.

STACKUP & IMPEDANCE REPORT

DFM Engineer: John Macanas

Job Name: 53929
Customer : SAMTEC INC
Part Name: PCB-112938-SIG-XX
Rev: 00

Customer Required Finished Thickness: 63.000 (± 6.300) mils
Estimated Finished Thickness: 62.656 mils (Over mask on plated copper)
Estimated Over Lam Thickness: 58.456 mils

Lyr	Vendor	Image
CM		0.700 mils
L1	Oak Mitsui EMC	2.000 mils SIG Base Cu: 0.50 oz 0.600 mils HTE 10%
	EMC	3.064 mils Dk: 3.80 EM-827 1080 (65.0%)
L2		1.200 mils P/G Base Cu: 1.00 oz RTF 97%
	EMC	3.000 mils Dk: 3.83 EM-827 (1-1080)
L3		1.200 mils P/G Base Cu: 1.00 oz RTF 97%
	EMC	6.164 mils Dk: 3.80 EM-827 1080 (65.0%)
	EMC	Dk: 3.80 EM-827 1080 (65.0%)
	EMC	28.000 mils Dk: 4.40 EM-827 (4-7628) FILLER CORE
	EMC	6.164 mils Dk: 3.80 EM-827 1080 (65.0%)
	EMC	Dk: 3.80 EM-827 1080 (65.0%)
L4		1.200 mils P/G Base Cu: 1.00 oz RTF 97%
	EMC	3.000 mils Dk: 3.83 EM-827 (1-1080)
L5		1.200 mils P/G Base Cu: 1.00 oz RTF 97%
	EMC	3.064 mils Dk: 3.80 EM-827 1080 (65.0%)
L6	Oak Mitsui	2.000 mils SIG Base Cu: 0.50 oz 0.600 mils HTE 10%
SM		0.700 mils

DRILL TABLE

Start Layer	End Layer	Drill Type	Plate Type	Via Fill	Stacked Via	Min Drill Size (mils)	Drill Depth (mils)	Pad Size (mils)	Hole Qnty	Do Not Hit Layer	Related Process
1	6	Mechanical	PTH	----	----	0.000	58.5	0.000	0	----	Final Assembly - 1/6
1	2	Laser	Micro Via	Copper Fill	No	6.000	3.7	0.000	0	----	Final Assembly - 1/6
6	5	Laser	Micro Via	Copper Fill	No	6.000	3.7	0.000	0	----	Final Assembly - 1/6
1	3	Laser	Micro Via	Copper Fill	No	10.000	7.9	0.000	0	----	Final Assembly - 1/6
6	4	Laser	Micro Via	Copper Fill	No	10.000	7.9	0.000	0	----	Final Assembly - 1/6

	Plating Type	Panel Size	Grain Direction
Final Assembly - 1/6	Pattern Plate	18 x 24	18

Figure 2: Typical stackup and drill definitions of the board. The nominal dimensions and materials are shown for the first build.

Within practical limits, the same board construction can be built not only with different laminates, but also with different stackup-number targets. Some of the main stackup option considerations are summarized later.

Materials

The first boards were built with the same kind of laminate throughout all of the layers, EMC EM-827, which is considered to be equivalent to Isola 370HR, the popular low-frequency laminate. *Figure 3* shows the major mechanical and electrical properties of the laminate

Elite Material Co., Ltd.
http:\\www.emctw.com

Technical Data

High Tg / Low CTE / Lead Free
EM-827 / EM-827B

- Low Z-axis CTE < 3.0% (50~260℃)
- Excellent thermal stability for lead-free processing
- For general application

Basic Laminate Property

Property	Item		IPC-TM-650	Test Condition	Unit	Typical Value
Thermal	Tg		2.4.25	DSC	℃	175
			2.4.24	TMA	℃	160
			2.4.24.4	DMA	℃	185
	CTE, X/Y-axis		2.4.24.5	< Tg, TMA	ppm/℃	12/15
	CTE, Z-axis		2.4.24	< Tg, TMA	ppm/℃	45
				> Tg, TMA	ppm/℃	225
	Z-axis Expansion		2.4.24	50~260℃	%	2.6
	Td		2.4.24.6	TGA (5% W.L)	℃	350
	T288		2.4.24.1	Clad	Min.	20
				Etched	Min.	>30
Electrical	Dk (R/C: 50%)	1 MHz	2.5.5.9	C-24/23/50	-	4.8
		1 GHz			-	4.2
	Df (R/C: 50%)	1 MHz	2.5.5.9	C-24/23/50	-	0.018
		1 GHz			-	0.019
	Volume Resistivity		2.5.17.1	C-96/35/90	MΩ-cm	$>10^{10}$
	Surface Resistivity		2.5.17.1	C-96/35/90	MΩ	$>10^{9}$
Physical	Water Absorption		2.6.2.1	E-1/105+D-24/23	%	0.12
	Peel Strength (HTE)	0.5 oz	2.4.8	As Received	lb/in	6.5
				After Thermal Stress	lb/in	6.5
		1.0 oz	2.4.8	As Received	lb/in	8.5
				After Thermal Stress	lb/in	8.5
	Flexural Strength	Warp	2.4.4	As Received	MPa	460~500
		Fill		As Received	MPa	390~430
	Flame Resistance		UL-94	A & E-24/125	-	V-0

Rev: 2017 Aug.

Figure 3: *EM-827 material properties.*

Construction, stackup and material options

As will be shown later, there are plated-through hole arrays in two of the sections and blind via arrays in three of the sections. One section has various combinations of reference vias, both blind vias and through vias. There are no buried vias in the board and no sequential lamination is required, unless a stackup variant is used with very different core laminates, either much thinner, or much thicker. In the former, the laminate itself may require sequential processing; in the latter reaching layer 3 from the top or layer 4 from the bottom may not work with blind vias.

The thin outer prepreg allows us to keep the low-cost foil construction and use laser-drilled blind vias as long as the smallest-pitch via array can accommodate the L1-L3 and L6-L4 skip vias, which normally would be limited by the maximum allowed aspect ratio.

The current construction allows stackup variants with thinner L2-L3 and L4-L5 cores and/or heavier copper on those cores. In addition to different copper thicknesses, different copper types and/or different roughness values can also be used, though roughness is usually considered of secondary importance in power distribution networks. For easy comparison across different builds, the overall board thickness can be held constant while using different laminate thickness and copper weight options by adjusting the thickness of the middle prepreg accordingly. Alternately, the total board thickness can also be made different on purpose, if the user wants to study and correlate via structures reaching to various depth.

Board finish and silkscreen

Though this board does not assume any soldered assembly, and in general it may have very little direct influence on the power distribution performance of the board, passivation of exposed copper is still recommended. The board was built with flash gold surface finish. The exposed dielectric on the board surface is covered by the customary green solder mask; again, since this board is primarily for lower-frequency PDN tests, the solder mask has very little influence on the performance in that frequency range. To help to locate various structures during measurements, the board has silkscreen on the top and bottom. In the board file each group of vias has a reference designator and the vias have pin IDs assigned.

Finally, the surface has a thieving pattern that covers all unused areas. The thieving pattern for this board is small diamond shapes, but as long as the size of each copper feature is much less than the wavelength, the size and shape will not matter. *Figure 4* illustrates these features.
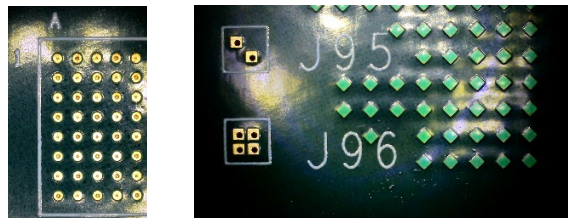
Figure 4*: Illustration of gold surface finish, green solder mask, silk screen for via arrays and reference patterns and thieving pattern on the outer layers of the board.*
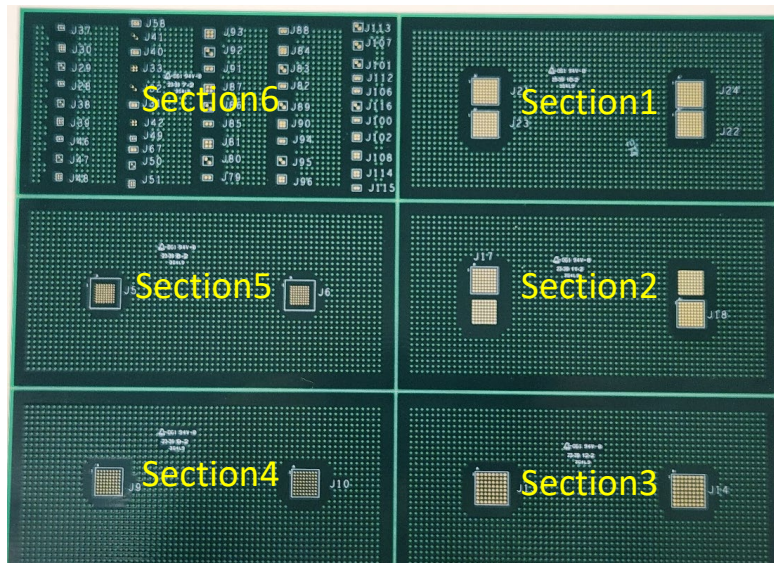
Layout
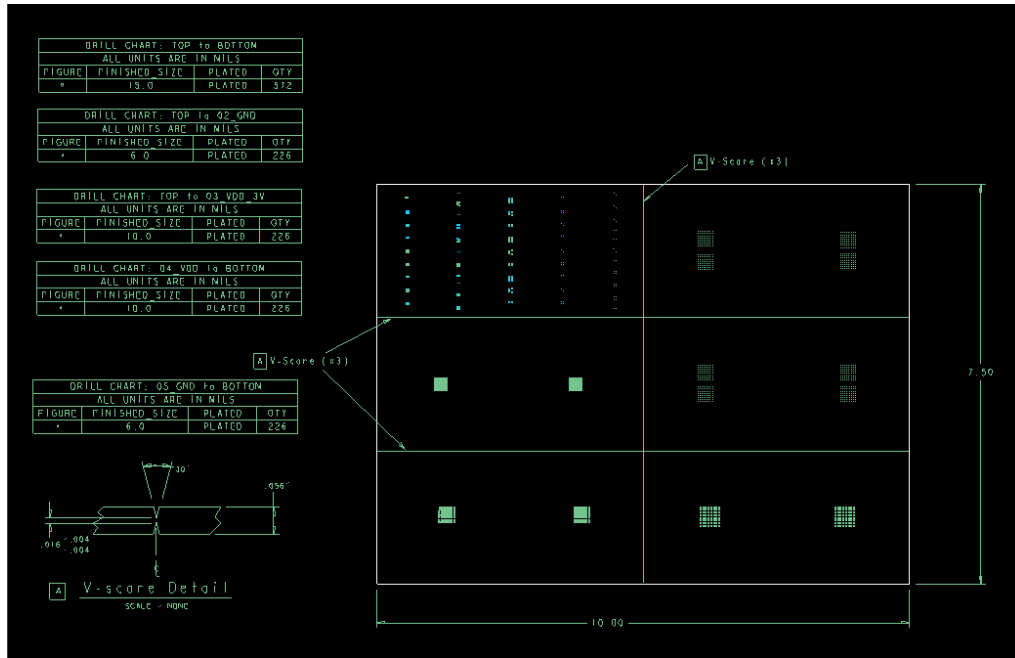
Figure 5*: Fab drawing detail, showing the outer dimensions (10"x7.5").*

The fab drawing image in *Figure 5* shows that within the 10"x7.5" envelope, there are six sections with identical plane sizes on L2, L3, L4 and L5. The planes in each section are 4.925"x2.425" in size. The six sections, numbered clockwise, are referred to as Section1 through Section6, as shown in *Figure 6*.

Figure 6*: Top board view, numbering of the six sections.*

Sections 1 through 5 have 8x8 via arrays with different via pitches, different connections, and different technologies. Section 6 is a reference section, with two or four vias using the plane connections and via technology that we have in Sections 1 through 5. *Figure 7* is the top view of a 1-mm plated through hole array. Pin A1 is connected to GND in all arrays, from there the pins follow a checker-board pattern and alternate between power and ground.

Figure 7: 8x8 via array on Section1 through Section5.

Overview of sections

While each section serves a useful purpose, this document focuses on two sections, Section 2 and its corresponding reference features in Section 6.

Section 1
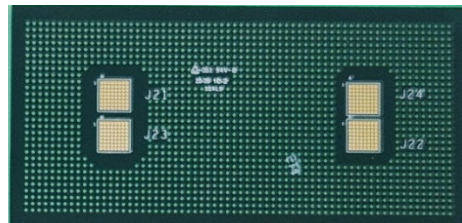
Figure 8: Top view of Section1, holding four 1-mm plated through hole arrays.

In Section 1, all four via arrays, with reference designators J21, J22, J23 and J24 are connected to both plane cavities, thus allowing us to look at vertical attenuation patterns in PDNs. Note that in this section all four via arrays are interconnected together through the planes.

Section 2
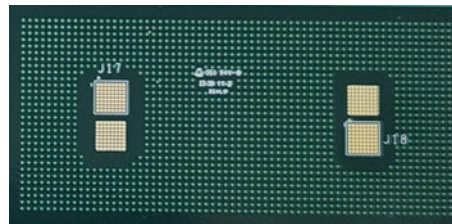
Figure 9: Top view of Section2, holding four 1-mm plated through hole arrays.

As shown in *Figure 9,* in Section 2 there are four 8x8 via arrays: J17, J18, J19 and J20. J17 and J18 connect to the L2-L3 plane cavity, whereas J19 and J20 connect to the L4-L5 plane cavity. The via pitch is 1mm (approximately 40 mils), same as in Section1, the padstack for the through via is captured in *Figure 10.* Note that because all four arrays use through holes, all four arrays are accessible from both the top and bottom side, but the two sets of two via arrays are not connected together.
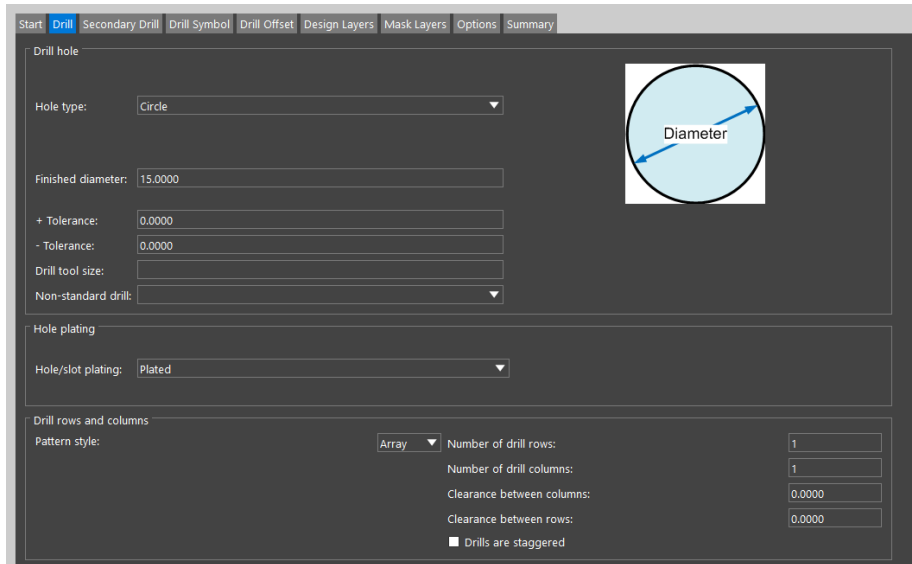

Figure 10: Via and padstack definition of the 1mm plated through hole arrays.

Section3, Section4 and Section5

These three sections use blind vias. Each section has four via arrays, two on the top, connecting to L2 and L3 and two on the bottom, connecting to L4 and L5. Section3 uses 50-mil (1.27mm via pitch, whereas the via pitch in Section 4 and 5 is 1mm and 0.8mm, respectively, see *Figure 11.*

Because the blind vias do not go through the board vertically, we can place the via arrays at the same X-Y location. Note that as long as we keep the stackup symmetric and balanced, the two via arrays on the top and on he bottom should behave identically. The reason for the duplication is that it allows us to do redundant measurements.
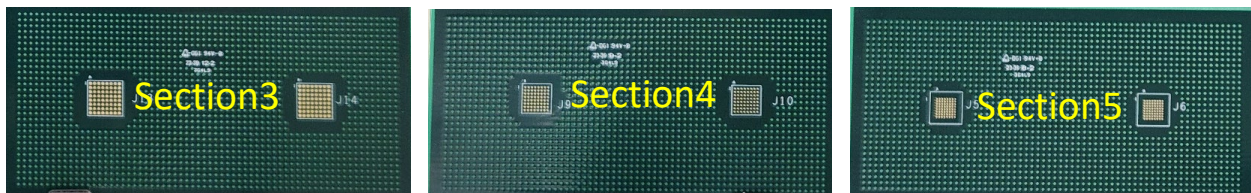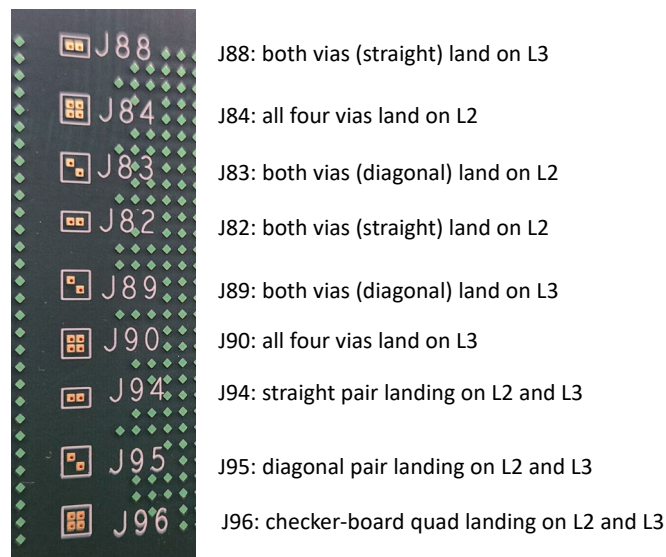

Figure 11: Sections3, 4 and 5 top view.

Section 6, reference

Section 6 has the various via types, sizes and pitches that are used on Section1 through Section5 in groups of two and four vias, making it simpler and easier to measure and correlate. Also, most of the reference vias connect intentionally to the same planes, which allow us to analyze shorter and longer via loops, without the added complexity of a plane cavity. As shown in Figure 12, the reference vias arranged in Section6 in five columns, corresponding to the five sections with different via arrays.
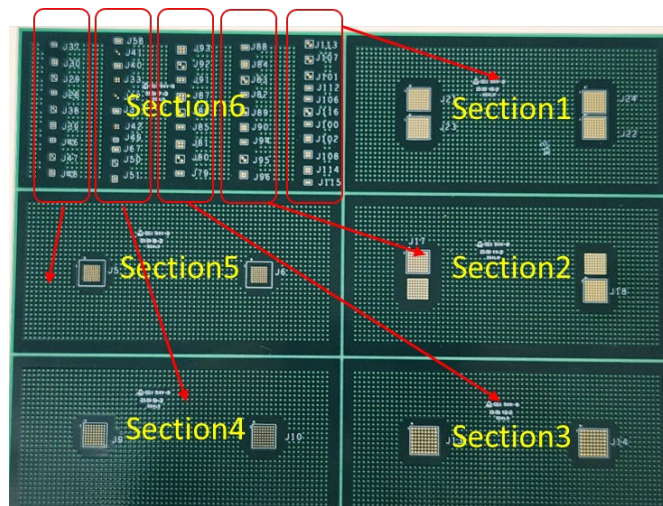

Figure 12: *Five columns of reference vias in Section6.*

Figure 13 shows the connectivity of each of the nine reference via groups.

J88: both vias (straight) land on L3

J84: all four vias land on L2

J83: both vias (diagonal) land on L2

J82: both vias (straight) land on L2

J89: both vias (diagonal) land on L3

J90: all four vias land on L3

J94: straight pair landing on L2 and L3

J95: diagonal pair landing on L2 and L3

J96: checker-board quad landing on L2 and L3

Figure 13: *Connectivity in the reference via groups referring to Section2.*

Focus area

Section2 offers the opportunity to probe via arrays that are connected to one plane cavity only. Moreover, the through vias allow us to probe in various configurations. To name a few obvious choices: we can probe at the selected via pair from top to bottom, at adjacent or more distant neighbor via pairs from the same side, either top or bottom. The spatial effect can be looked at by probing the structure at different locations, for instance at the corner, center and at the mid point of a side. The suggested locations in Figure 14 also give the possibility to get transfer parameters between more distant locations.
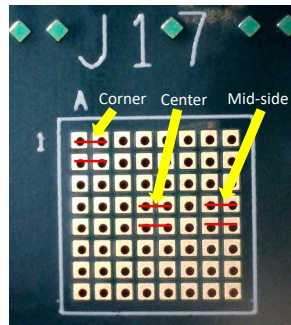
Figure 14: Suggested port locations for Section2 J17 measurements and simulations.

If we probe power-ground vias in the via arrays with nothing attached to the board, we actually probe an open-terminated plane cavity, which represents capacitive reactance at low frequencies. At high frequencies, where the modal resonances of the planes develop, we could also collect information about the dielectric properties. If we limit ourselves to frequencies below the modal resonances, we need a shorted structure so that we can assess the resistance and inductance of the structure. We can solder a shorting plane over the second via array on the planes, in this case J18, but it may require a professional BGA soldering station to do it properly and repeatably. Alternately, we can easily create removable shorts by clamping a carefully flattened copper sheet, cut to the proper size, over the entire via array of J18. To make sure that the connection is repeatable, we can apply silver paste on the shorting copper sheet.

To complement the data that we can collect on the via arrays, the reference via groups offer further correlation opportunities as several of them create directly shorted conductive path, without the need to go through the plane cavity and the second via array to create a closed loop. For instance, we can measure the via group in J84 in different configurations, preferably with the same port orientation and port assignment that we use for the three locations at J17 (see Figure 15). The four vias in J84 can be considered as a cutout from J17 at the three selected locations, the only difference being that all four vias are connected to L2, shorting them together. Even though we have only four vias in the group, this structure, just like several of the other reference via groups, offers a large number of possible permutations to simulate and/or to measure. Note that via group J90 similarly connects all four vias to the same plane, but it is L3 instead of L2.
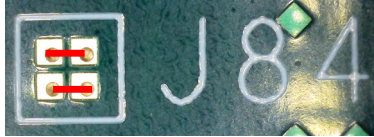
Figure 15: *Suggested port orientation for measurements and simulations in Section6 J84.*

Acknowledgement

Summary

Eventually, when the design becomes open source, the goal is to make available the following material:

- Native Allegro board file, Gerber files, ODB++ files and IPC2581 files
- Schematics file in native Cadence format, as well as in industry standard IPC-356 and pdf formats
- Material and stackup definitions of the manufactured boards
- Sample measurement data on Section2 and Section6
- Sample simulation data on Section2 and Section6

The documentation will enable users to fabricate the benchmark boards themselves, either in its default construction or in any variant of it. The default benchmark board may also become available for purchase.

In addition to the documentation, script(s) to analyze, compare and post-process measured and simulated data may also become available in the future.

References

[1]   IEEE EPS TC-EDMS Packaging Benchmark Suite, 2021. [Online]. Available: https://packaging-benchmarks.org

[2]   Heidi Barnes, et al, "The IEEE EPS Packaging Benchmark Suite," IEEE 2022

[3]   Ethan Koether, et al, "3D Connection Artifacts in PDN Measurements," DesignCon 2023

[4]   Ethan Koether, et al, "Impact of Finite Interconnect Impedance including Spatial and Domain Comparison of PDN Characterization," to be published at DesignCon 2024