PCB Design 007 *QuietPower* columns, August 2010

Inductance of Bypass Capacitors, Part III
Loop or mounted inductance

Istvan Novak

The previous column, *Inductance of Bypass Capacitors, Part II*, showed the current loop formed by a multi-layer ceramic capacitor attached to a printed circuit board. We now start with the same figure to explain the possible different definitions when it comes to the inductance of bypass capacitors. In this column we look at the *loop inductance*, also called the *mounted inductance*.

The capacitor is shown mounted to surface pads on the PCB. For sake of simplicity, only those two layers are shown in the board, where the capacitor is connected.

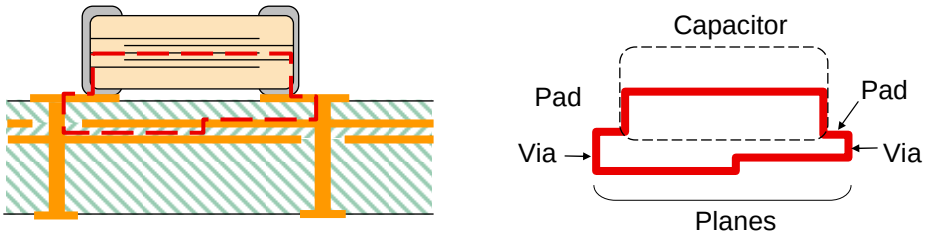

Figure 1: *On the left: side cross section view of a mounted bypass capacitor*. On the right: contributors to the loop inductance. The red line represents the current loop.

The easiest to understand is the definition when we consider the inductance along the entire loop. This is called (no surprise) *loop inductance.* Sometimes it is also called *mounted inductance*, because it gives the full inductance of the device mounted on a given user geometry. Loop inductance is important, for instance, when we need a reasonably accurate estimate for the Series Resonance Frequency (SRF), or for the anti-resonance peaking between two different-valued capacitors or between the capacitor's inductance and the static capacitance of the power/ground planes it connects to. Unfortunately the mounted inductance is not a unique property of the capacitor; it strongly depends on the user geometry (escape traces, pads, via patterns) as well.

Figure 2 is a simulated illustration of such an anti-resonance between a 1uF 10 mOhm bypass capacitor mounted in the middle of a 5"x5" FR4 plane pair with 10-mil dielectric thickness with two different mounted inductance values: 1 nH (blue trace) and 3 nH (green trace). The black trace shows the impedance of the planes without the capacitor. There is very little difference with the different mounted inductances at low and at high frequencies. At low frequencies the impedance is dictated by the capacitive reactance of the 1uF capacitor. At very high frequencies the impedance is determined by the modal resonances of the planes.

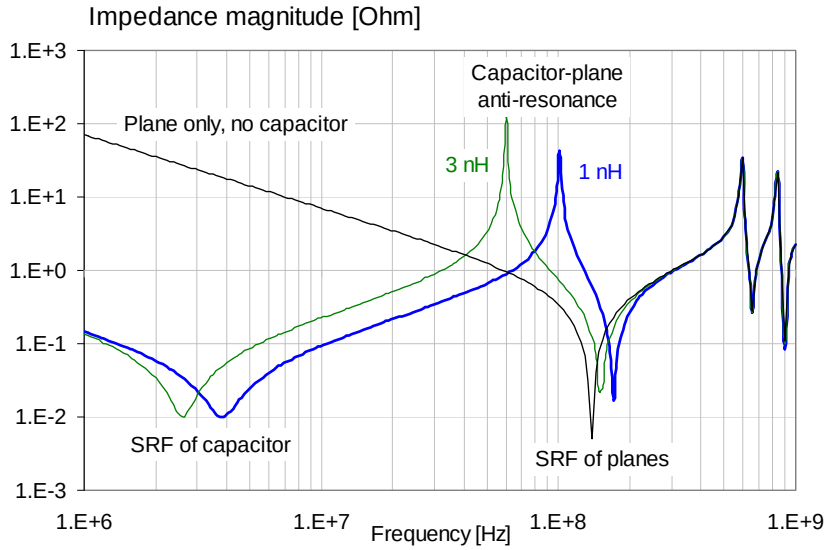

Figure 2: *Anti-resonance between the capacitance of a power-ground plane pair and a bypass capacitor with 1 nH or 3 nH mounted inductance.*

In this case, the mounted inductance matters over about two decades of frequencies and higher mounted inductance of the capacitor shifts all three resonance frequencies to lower values. SRF of the capacitor is an important parameter for multi-pole impedance approximation, when we line up the SRFs of different-valued capacitors along the frequency axis. The capacitor-plane anti-resonance is important because (as the figure also illustrates it), higher mounted inductance results in higher Q and higher peak impedance value. So from a design point of view, it is important and very useful to know the mounted inductance of the part.

Measuring the mounted inductance directly is not easy. We can, however, easily measure the mounted inductance indirectly at two discrete frequencies, by back-calculating it from SRF or from the static plane capacitance and the frequency of the capacitor-plane anti-resonance. We can measure the static plane capacitance without any component attached to the planes; in the example circuit of *Figure 2* it is approximately 2.4 nF. We can then mount the capacitor and measure the frequency of the anti-resonance. The blue trace on the figure has an anti-resonance peak at 100 MHz. From this peak frequency and the 2.4 nF static plane capacitance the calculated loop inductance comes very close to 1 nH.

$$f_0 = \frac{1}{2\pi\sqrt{L_{mounted} C_{plane}}} \qquad L_{mounted} = \frac{1}{4\pi^2 f_0^2 C_{plane}}$$

In the next columns we will look at other possible inductance definitions for the bypass capacitors.