PCB Design 007 *QuietPower* columns, September 2010

Inductance of Bypass Capacitors, Part IV
Don't double count plane inductance

Istvan Novak

The previous column, *Inductance of Bypass Capacitors, Part III*, introduced the *loop inductance*, also called the *mounted inductance*. In this column we show that loop inductance not only depends on the user geometry, but also when used in simulations, it double counts the plane inductance.

As a reminder, we start again with the side view of a capacitor attached to a PCB and its associated current loop.

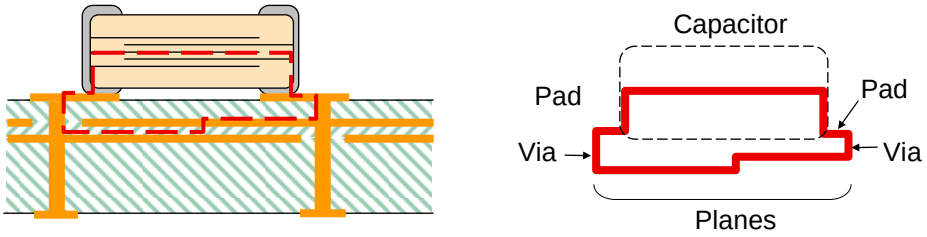

Figure 1: *On the left: side cross section view of a mounted bypass capacitor. On the right: contributors to the loop inductance. The red line represents the current loop.*

Imagine now that we want to simulate the behavior of the capacitor together with a pair of PCB planes. An accurate, brute force, and for most applications unnecessary, solution would be to use a full-wave solver with the entire geometry included. This approach usually takes too long to solve and therefore we often approximate the solution in circuit simulators, for instance SPICE.

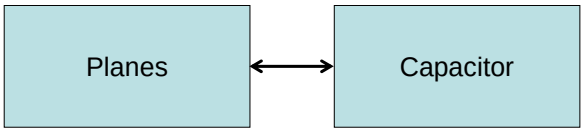

Figure 2: *Equivalent circuit of a single capacitor together with power planes*

When we use the circuit simulator approach, we have a block describing the planes, and another block describing the capacitor. Lets assume we have only the mounted inductance available for the capacitor. If we also know the capacitance and ESR of the part, we can use the familiar series C-R-L equivalent circuit as shown in *Figure 3*.

Figure 3: *A possible equivalent circuit for the bypass capacitor, using the mounted inductance*

Plane pairs can also be described with circuit equivalents, for instance a grid of transmission lines. *Figure 4* shows a simple equivalent circuit for rectangular planes.

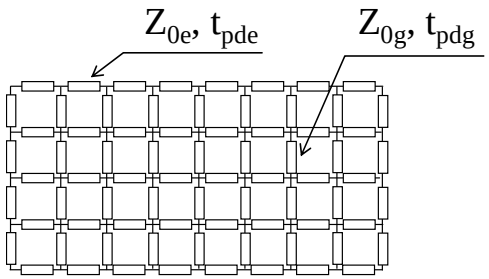

Figure 4: *A possible equivalent circuit for a pair of rectangular planes. Z_0 and t_{pd} represent the characteristic impedance and propagation delay of the transmission line segment, respectively. Suffix 'g' and 'e' refer to 'grid' and edge' segments, respectively.*

If you are not familiar with this plane equivalent circuit, don't worry. In later columns we will look in more details at various ways to simulate planes, including this transmission-line equivalent circuit.

Once we select the grid node on the plane model, which represents the location of the capacitor, we are ready to connect together the equivalent circuits of *Figure 3* and *4*, to implement the block schematics shown in *Figure 2*. And here comes the problem: any reasonable plane model (the one in *Figure 4* is no exception) will capture not only the distributed capacitance but also the inductance of the planes. As a first approximation, each miliinch plane spacing comes with approximately 33 pH inductance. This means by using the mounted inductance for the capacitor, the plane inductance is included twice: once in the capacitor model and once in the plane model. **If we use the mounted inductance for the capacitor to simulate it with planes, we double count the plane inductance.**

How much error this double-counting creates, it depends on the geometry. Mounted inductance dominated by plane inductance will show the biggest error, ultimately almost doubling the inductance. Since the resonance frequency scales with the square root of inductance, the capacitor's resonance frequencies will shift to lower values by as much as

40%. This happens when the vertical distance between the planes is big compared to the via-pad-capacitor portion of the current loop.

The other extreme, resulting in minimal error, is when the capacitor connects to tight planes with long vias and/or escape traces. These two cases are illustrated in *Figure 5*.

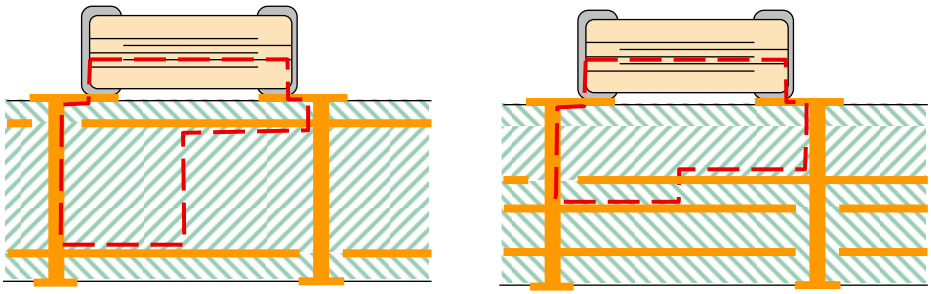

Figure 5: Illustration of loop-size error for double counting. Left: far spaced planes and short vias outside. Right: tight planes, long vias/escapes

Note that this potential double counting does not depend on the type of capacitor model we use. Whether it is a fitted rational macromodel, or S parameter block, or a series C-R-L model, if it describes the behavior of the mounted capacitor, by connecting it to a plane model, we double count the plane inductance.

Conclusion: if all what we have for the bypass capacitor is mounted inductance (for instance, from measurements), we need to subtract from it the approximate plane inductance value before we use the capacitor and plane models together.